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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/523,239

09/28/2005

Franz Schuler

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6476

48581 7590 01/14/2008  
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EXAMINER

SALERNO, SARAH KATE

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

01/14/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

## Application No.

10/523,239

## Applicant(s)

SCHULER ET AL.

## Examiner

SARAH K. SALERNO

## Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 7-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/S508)
- Paper No(s)/Mail Date 01/19/05
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I, claims 1-6 in the reply filed on 11/28/07 is acknowledged.
2. Claims 7-14 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of fabricating a semiconductor component, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/28/07.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Joy et al. (US Patent 4,454,647).

Claim 1: Joy teaches a semiconductor component with trench isolation for defining active regions in a semiconductor substrate, the trench isolation comprising (FIG. 4): a deep isolation trench with a covering insulation layer (14),

a side wall insulation layer (28) and an electrically conductive filling layer (30), which is electrically connected to a predetermined doping region of the semiconductor substrate (2) in a bottom region of the isolation trench; and further comprising:

a trench contact (30), which comprises a deep contact trench with a side wall insulation layer (28) and an electrically conductive filling layer (30), which is likewise electrically connected to the predetermined doping region of the semiconductor substrate (30) in a bottom region of the contact trench.

Claim 2: Joy teaches the covering insulation layer (14) is formed essentially below a surface of the semiconductor substrate (2-4) and within the isolation trench (FIG. 4).

Claim 3: Joy teaches the trench isolation (28) and the trench contact (30) have a larger depth than an associated depletion zone in the semiconductor substrate (2-4) (FIG. 4).

Claim 4: Joy teaches the trench isolation further comprises a widened, shallow isolation trench (14) at a surface of the semiconductor substrate configured for filling non-active regions (FIG. 4).

Claim 5: Joy teaches the predetermined doping region comprises a doping well comprising a multiple well structure (2-4) (FIG. 4).

Claim 6: Joy teaches the semiconductor substrate comprises Si (Col. 4 lines 5-6), the covering insulation layer (14) and side wall insulation layer (28) comprise SiO<sub>2</sub> (Col. 5 lines 10-20, 32-35; Col. 6 lines 29), and the filling layer comprises highly doped polysilicon (Col. 6 lines 50).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./  
Examiner, Art Unit 2814

/Theresa T. Doan/  
Primary Examiner, Art Unit 2814